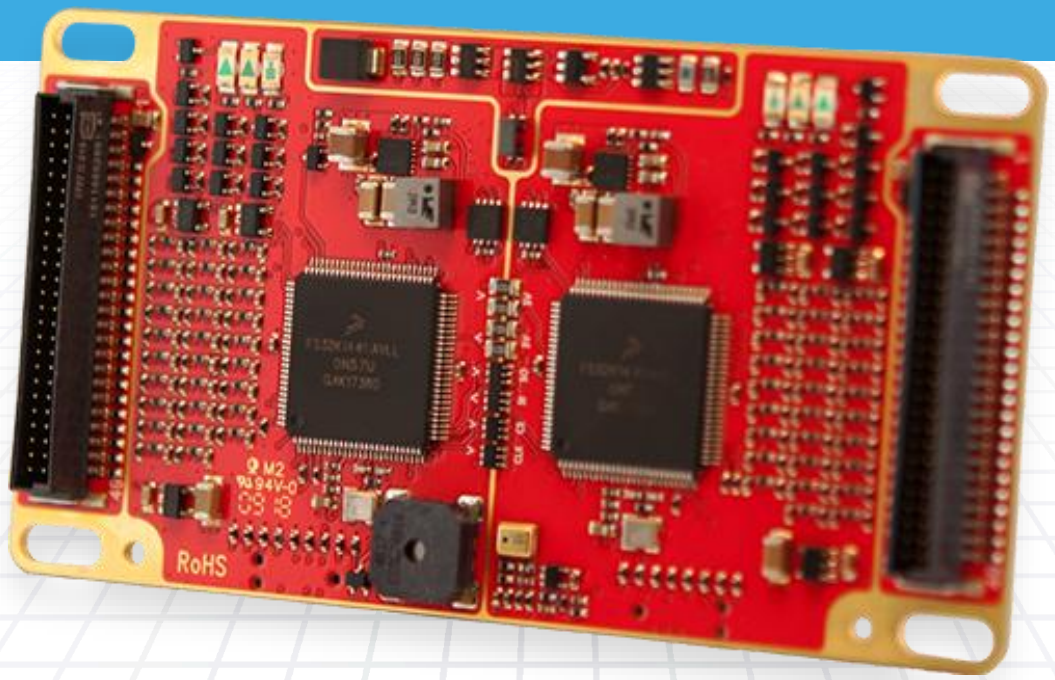
SCM

SAFETY CABIN MODULE
PRODUCT MANUAL



The SCM is responsible for gathering user input from joystick, switches etc. and controlling LED's.
The module communicates with the system using CAN J1939.
This module operates as a CAN slave device, it intended to be controlled by a CAN master device and can interface with the majority of the mobile CAN master devices available on the market today.
The targeted industry includes but is not limited to forestry, construction and agricultural machinery.
The SCM is designed according to ISO 13849-1, performance level D, Category 3.

ELECTRUM AUTOMATION AB
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SCM Overview

Typical applications includes

- Armrest assembles
- Joystick assemblies
- Dash panels
- Remote controls

Technical data

- Input voltage range 9 - 35V_{DC} operational supply voltage
- Designed to be assembled in a board-to-board configuration
- Two 50p male Harting HAR-Flex connectors
- A total of 52 Analog or digital inputs which can be used for sampling safety related signals
- A total of 20 PWM outputs
- A total of 2 SPI communication ports for expansion up to 192 digital I/O
- A total of 6 +5V supply rails with independent supervision
- Built in 90dBA speaker with microphone supervisor
- Operating ambient temperature -40° to +85°C

Mechanical data

- Dimensions: 95x50x8.3mm
- Total stacking height of 9.6mm measured as height added

Communication

- Hardware support for CAN 2.0A, CAN 2.0B and CAN FD
- J1939 proprietary CAN protocol. One single SCM presents itself as two nodes on the CAN bus
- Customized CAN protocols are available on request

Test standards

- Immunity conducted interference ISO7637-2, pulse 1, 2a, 2b, 3a, 3b, 4, pulse 5: +123V
- Immunity to interfering fields ISO 11452-2, 200MHz-2GHz, 100V/m
- Current injection ISO 11452-4, 20MHz-200Mhz, 100mA
- Interference emission EN ISO 13766 1:2018, 30 MHz – 1 GHz
- ESD ISO 10605, 8kV contact, 16kV air

Safety standard

- Designed according to ISO 13849-1 PLd, Category 3

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1 About this document

1.1 Introduction

The instructions in this manual are to be used as a reference tool for the machine manufacturer's design, production, and service personnel to ensure a proper integration of the SCM module.

The user reading these instructions should have basic knowledge in working with electronic equipment.

The latest version of this document is available at www.electrumab.se

1.2 Terms, definitions and abbreviated terms

1.2.1 SCM

SCM refers to Safety Cabin Module, this is the product manual for the SCM module.

1.2.2 CAN master

The CAN master refers to the CAN device which will be receiving and evaluating the data which the SCM module transmits on the CAN bus.

1.2.3 Mother-board

The use of the term mother-board in this document refers to the PCB board which the SCM module will attach to.

1.2.4 Channel

The use of the term channel in this document refers to a redundant hardware/software channel. The SCM module consists of 2 channels in order to comply with ISO 13849-1 Category 3.

1.2.5 CHx_OBJECTz

The use of the term x and z is used throughout this document to identify all objects of the same kind, x refers to channel 1 and channel 2 and z refers to the instance number.
Example:
CH**x**_AI**z** refers to both channel 1 and 2, z refers to all analog input instances (1-16).

1.3 Symbols

1.3.1 Safety Requirement

Sections in this document which defines a functional safety requirement are identified with a yellow box containing a warning icon, requirement identifier, header and description.

SREQ 0001	***Example of a functional safety requirement***
	This is a functional safety requirement. Read and make sure you understand and comply with this requirement.

2 Precautions

SREQ 0002	*All functional safety requirement shall be fulfilled*
	All functional safety requirements stated in this manual shall be fulfilled if the product is intended to be used in a safety related application.

SREQ 0003	*Use within specification*
	The product shall only be used within its specified range.

3 Electrical characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Operational voltage(1)		9		35	V_{DC}
Power consumption Idle(2)	35V < VIN > 9V	0.6	0.7	0.9	W
Operating temperature		-40		85	°C
Analog input voltage range	On any analog/digital input	0		5	V_{DC}
Digital input voltage hysteresis	Low -> High		2.6		V
	High -> Low		2.4		V
Analog voltage input impedance	Fixed pull-down	99k	100k	101k	Ω
PWM frequency	Fixed frequency		20		kHz
PWM duty-cycle		0		100	%
5V analog output voltage(3)		4.9	5.0	5.1	V
5V output current	CHx_5V_SPI and CHx_5V_OUTPUTS		500	1000(4)	mA
	CHx_5V_INPUTS		250	500(4)	mA

Note:
1. Module fully operational.
2. Module fully operational. No signals connected to SCM except for supply voltage and GND.
3. The ADC measurements are referenced to the same +5V potential as the analog output voltage.
4. It is not recommended to operate at maximum current consumption for longer periods of time due to excessive heat loss.

4 Speaker data

Parameter	Condition	Min.	Typ.	Max.	Unit
Speaker frequency			2.73		kHz
Sound pressure level	Open air, 10cm distance		90		dBA

5 Absolute maximum ratings

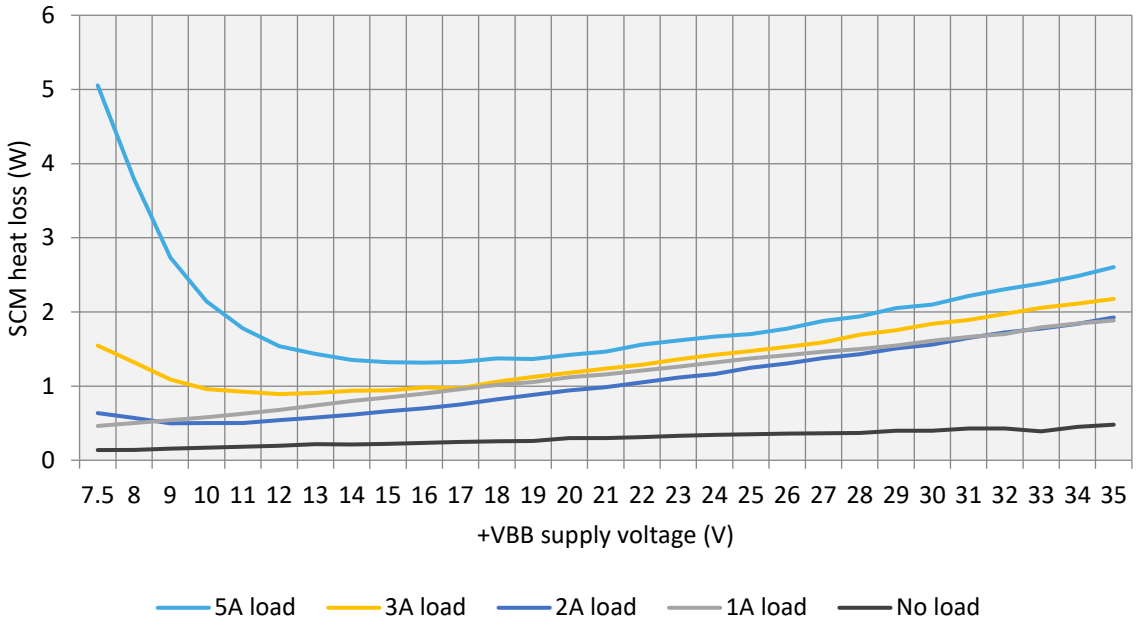
Parameter	Condition	Min.	Typ.	Max.	Unit
VBB input voltage(1)		-150		150	V_{DC}
Input voltage CANL & CANH (1)		-36		36	V_{DC}
Storage temperature(1)		-55		125	°C
Max input voltage other pins(1)	All other pins except CAN and VBB	0		5.5	V_{DC}

Note: 1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6 Heat loss

This graph illustrates the heat loss on the SCM board in relation to the output current and supply voltage. The measurement was performed with evenly distributed resistive loads on the 5V supply rails across both channels. Measurement accuracy is ±10%.

$P_{heat\text{-}loss} = P_{in} - P_{out}$



7 Functional safety data

The safety function of the SCM is to safely convert analog and digital signals and transmit the data over a single CAN bus. Only the analog inputs in the SCM board are safety classified. The digital outputs and SPI ports are **not** safety classified.
The safety principle of the SCM is based on redundancy, no single fault in the device shall lead to a dangerous state. The SCM uses the de-energization principle described in ISO 13849-1, this means that the SCM module shall **not** be used in safety applications which require constant operation, for example steering-by-wire at high speeds.
The safe state of the system shall always be to restrict or disable any dangerous movements in case the SCM **or** the CAN master detects a fault.

SREQ 0004	***Safe state***
	This product shall only be used in systems which are in a safe state when the system is in a de-energized state. This product shall not be used where the safety function requires a constant operation.

SREQ 0005	***Safety functions***
	Only the CH**x**_AI**z** inputs of the SCM are safety classified. No other I/O on the SCM board shall be used for safety related functions.

SREQ 0006	***CAN master responsibility***
	This product is intended to be connected to a CAN master. The CAN master shall be responsible for making sure that the overall system safety integrity is guaranteed in the event of a fault.

SREQ 0007	***Expected restart interval***
	This product shall only be used in applications where it is expected to be shut down or restarted within 48 hours of startup.

Parameter	Note	Value
Safety standard		ISO 13849-1
Performance level[(1)]		PL d
MTTFD[(1)]	MTTFD for one channel	178.6 years
DCavg[(1)]		60%
Category		Cat 3
CCF		70 points
Safety response time		300ms
Mission time		20 years

Note: 1. In order to assure the safety integrity level claimed in this table the integrator of this module must ensure that the installation conforms to the safety instructions described in this manual

8 Handling

8.1 Mechanical sensitivity

The entire SCM is protected with a protective coating covering the majority of the components. Even so, the SCM board shall be protected against mechanical damage and must be handled with care. The SCM contains very small components and tracks. Physical damage to the SCM which are caused by reckless handling is not covered by warranty.

SREQ 0008	*Handle with care*
	This product shall be handled with care in order to avoid mechanical damages.

8.2 ESD

The SCM board is sensitive to electrostatic discharges, all handling of the SCM module shall take place in an ESD safe environment. All pins in the exposed connectors SCM board are protected against ESD.

The internal tracks/components on the SCM are **not** protected against ESD.
Damages to the SCM board which can be linked to ESD are not covered by warranty.

SREQ 0009	*ESD safety*
	All handling of the SCM board shall occur in an ESD safe area.

8.3 Installation, commissioning and maintenance

Installation, commissioning and maintenance of the SCM board shall be carried out by personnel with proper training. Personnel involved in installation, commissioning and maintenance shall be trained in such a manner that they do not contradict any of the requirements stated in this manual.
The SCM board itself does not require any maintenance. Modification or repair of the SCM shall not be carried out by third-party.

SREQ 0010	*Proper training*
	Personnel involved in installation, commissioning and maintenance shall be trained in such a manner that their actions does not contradict any of the requirements stated in this manual.

SREQ 0011	*Repair*
	A damaged product shall not be used and may only be repaired by Electrum Automation AB.

9 Warranty

In the event of a malfunctioning SCM module, the faulty SCM module shall be sent to Electrum Automation AB for further investigation.
If the fault can be tracked to improper handling or usage, Electrum Automation AB reserves the right to claim the customer for costs involved in the warranty process.

10 Board-to-board mount

The SCM board is intended to be mounted in a board-to-board configuration. This enables the SCM to become more flexible to external design changes. This will also result in a more suitable wiring harness to each sensor/switch/PCB board etc.
Below is an example of the mother-board layout which the SCM is intended to be attached to.
The example covers the placement of connectors, standoffs and a brief recommended routing. In the examples below 4pcs of Würth M3, 8mm standoffs are used (part.no 9774080360R) along with 2pcs of 50p Harting HAR-Flex female connectors (part.no 15210502601000).

The selected Harting HAR-Flex connectors on the mother-board shall have locator pins to ensure a proper alignment between the SCM and the mother-board.

Please note that the four M3 mounting holes are connected to the ground potential on the SCM board and shall be connected to ground potential on the mother-board as well.
4 pcs of regular M3 screws should be used. Maximum screw tightening torque is 0.5Nm.
Thread lock should be used in order to ensure a proper mount over time.

Please note that the size of the mother-board can not be smaller than the actual SCM (95x50mm).

The SCM board is protected against 180° mating error with the mother-board due to the use of connectors with mating keys. To improve the mating procedure of the mother-board and SCM module it is recommended to add circular holes to further clarify the rotation of the SCM board.

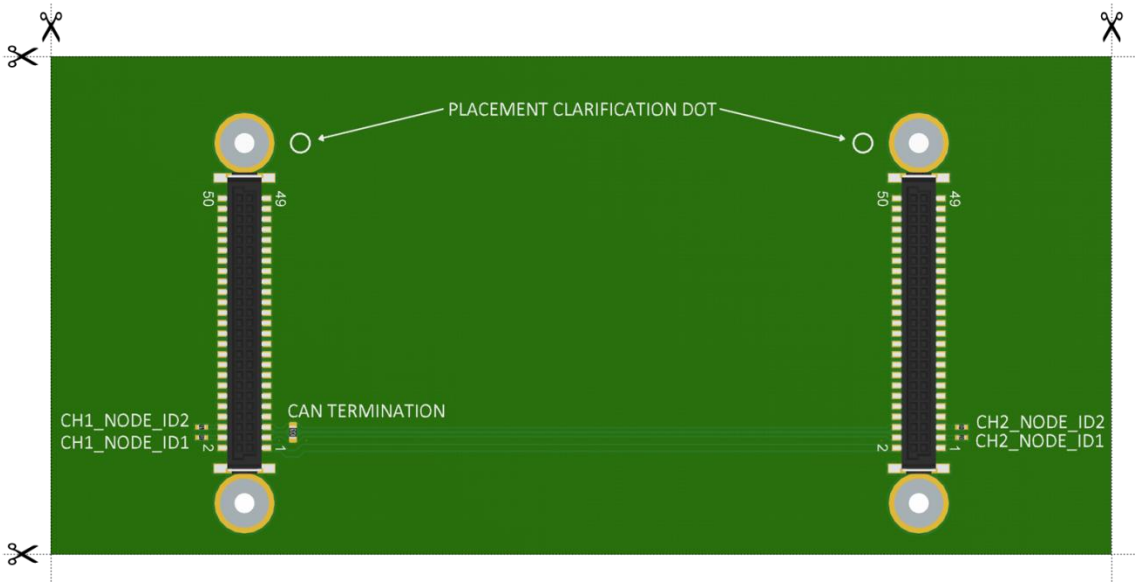
10.1 Connector manufacturer

The SCM is intended to interface with 2 pcs of 50p female connectors mounted on a mother-board. The SCM uses a generic connector family which is interchangeable between multiple manufacturers. The connectors used on the SCM is selected based on the current availability from the list of approved manufacturers in the table below.

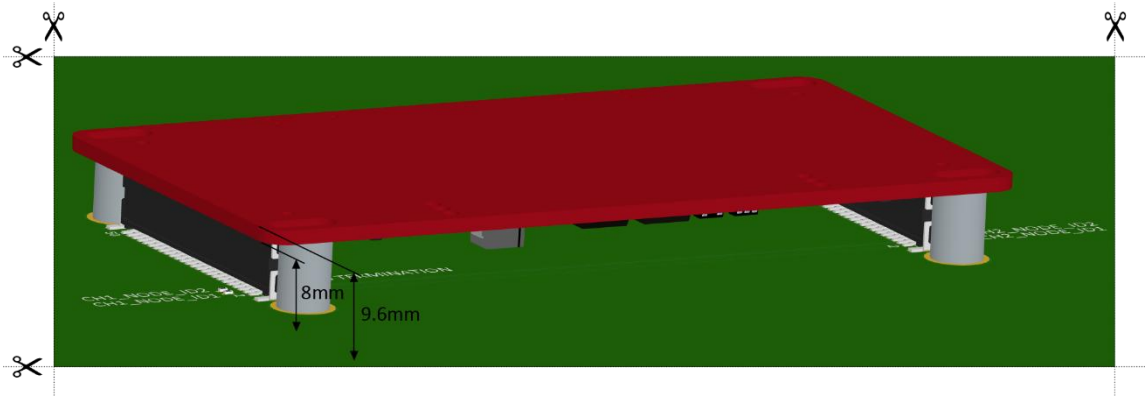
Manufacturer	Series	Male connector (SCM)	Female connector (mother-board)
Harting	HAR-Flex	15110502601000	15210502601000
Phoenix	FR	1373889	1374033

10.2 Mother-board Bottom side view

10.3 Mother-board Top side view

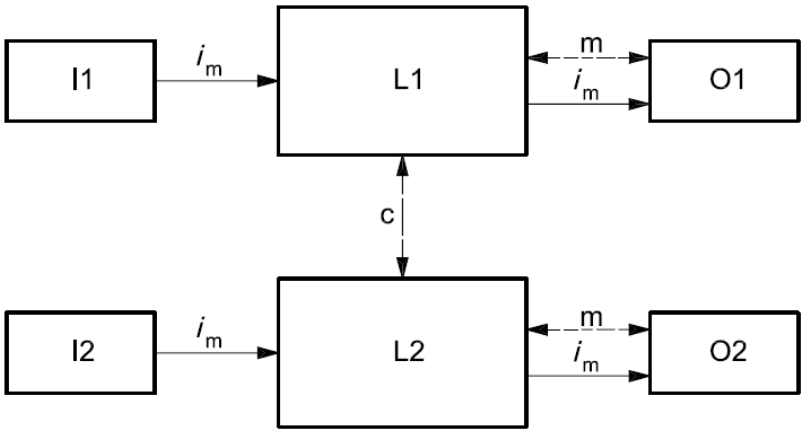


10.4 Board-to-board assembly 3D view



11 Safety principle

The SCM is constructed according to Category 3 in ISO 13849-1. This means that safety is achieved with the use of redundancy and cross monitoring. The figure below is an illustration of a Category 3 system. The figure derives from ISO 13849-1.



Key

i_m	interconnecting means
c	cross monitoring
I1, I2	input device, e.g. sensor
L1, L2	logic
m	monitoring
O1, O_2	output device, e.g. main contactor

Dashed lines represent reasonably practicable fault detection.

A common cause failure occurs when a single fault causes multiple faults as a consequence. No single fault shall be allowed to compromise the safety integrity of both channel 1 and channel 2.
Under no circumstance shall any signals be shared between the channels, for example by using a power rail from channel 1 to power an analog input on channel 2.

SREQ 0012	***Common cause failure***
	Any kind of signals between the two channels shall be examined thoroughly to reduce the risk of common cause failures. Any two adjacent tracks on any PCB which derives from channel 1 and channel 2 shall be separated by (at least) a ground potential.

12 +5V supply rails

The SCM module features a total of 6 +5V supply rails, 3 on each channel.
Each power rail features an independent supervision of the actual analog output voltage.
The SCM module is responsible for sampling each power rail and report the error on the CAN bus in case the power rail is outside of specification.
When designing the external loads connected to the power rails, care should be taken to evenly distribute the loads across the two channels, this will ensure that the SCM module operates without generating unnecessary heat.

The output voltage on the +5V rails for each channel are identical to the internal +5V supply voltage (not taking into account the $R_{DS\text{-}ON}$ of the overcurrent protection circuit which are attached in series with each supply rail).

SREQ 0013	***Usage of correct supply rail***
	All signals shall be powered from its intended power supply rail.

12.1 CHx_5V_INPUTS

Supply voltage for joysticks, switches etc. All CH**x**_AI**z** on the same channel shall be powered using this power rail. Under no circumstances shall any other power rail be used to supply the analog/digital inputs.
Each channel has the capability to supply 500mA current on this power rail.

12.2 CHx_5V_OUTPUTS

Supply voltage for LED's, buzzers etc. All CH**x**_DO**z** on the same channel shall be powered using this power rail. Under no circumstances shall any other power rail be used to supply the sinking digital outputs.
Each channel has the capability to supply 1000mA current on this power rail.

12.3 CHx_5V_SPI

Supply voltage for powering input/output shift registers which can be used to increase the number of I/O's on the PCB. All SPI devices on the same channel shall be powered using this power rail. Under no circumstances shall any other power rail be used to supply the external SPI devices.
Each channel has the capability to supply 1000mA current on this power rail.

13 Analog/digital inputs

13.1 Voltage reference

The analog/digital inputs are referenced to its corresponding channel +5V internal voltage. This means that the SCM automatically compensates for internal component tolerances if given the condition that ratiometric sensors are used.

Example: The CH1_5V_INPUTS supply rail which should in theory be +5.00V is actually +4.9V due to component tolerances. If CH1_5V_INPUTS is directly connected to CH1_AI1, the resulting CH1_AI1 ADC value will still read approximately 0xFFF (100% of a 12bit scale).

13.2 Resolution

The SCM reports all AI signals with a 12 bit resolution. 0x000 = 0V, 0xFFF = CH**x**_5V_INPUTS.

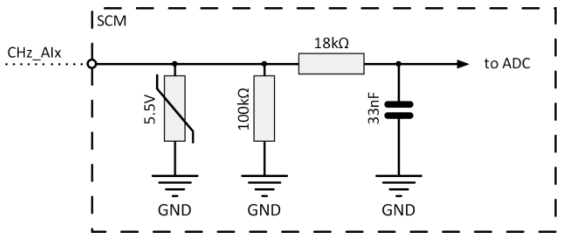
13.3 Input impedance

All CH**x**_AI**z** are internally connected to ground via a 100kohm resistor followed by a 268Hz low-pass RC-filter. If lower impedance is required an external pull-down resistor should be added on the mother-board.

13.4 Analog/digital input selection

The SCM samples all CH**x**_AI**z** as analog values, the software will treat all analog inputs which are above 3250mV as a 1 and below 1750mV as 0.
A digital filter with hysteresis is added as well to increase the resilience against switch debounce, ESD and RF fields.
The software will report all analog inputs in their digital interpretation on the CAN bus in a single CAN packet.

13.5 Internal diagram of an analog input



13.6 Safety considerations

SREQ 0014	*Safety inputs*
	For input signals which are considered safety related, a redundant set of signals shall be supplied. The redundant set of signals can be connected to any CHx_AIz as long as one signal is connected to channel 1 and the other to channel 2. Please note that the SCM module does not perform any signal integrity cross-check since the SCM module is a generic safety CAN slave without any knowledge of which signals are connected to each input/output. The task of performing the cross-check signal integrity shall be implemented and verified by the CAN master.

13.7 Example schematics

Please note that the schematics below are simplified and covers the typical applications which the SCM is intended for. More external components other than those displayed in the simplified schematic may be required.

SREQ 0015	*Usage of sensor/switches with complementary outputs*
	Sensor/switches with complementary outputs shall be used if there is a risk that the signal integrity from the redundant sensor/switches is subject to common cause failures, for instance short circuit between channels, ESD, RF field exposure etc. The redundant set of signals shall have a voltage sum of (approximately) +5V during normal operation.

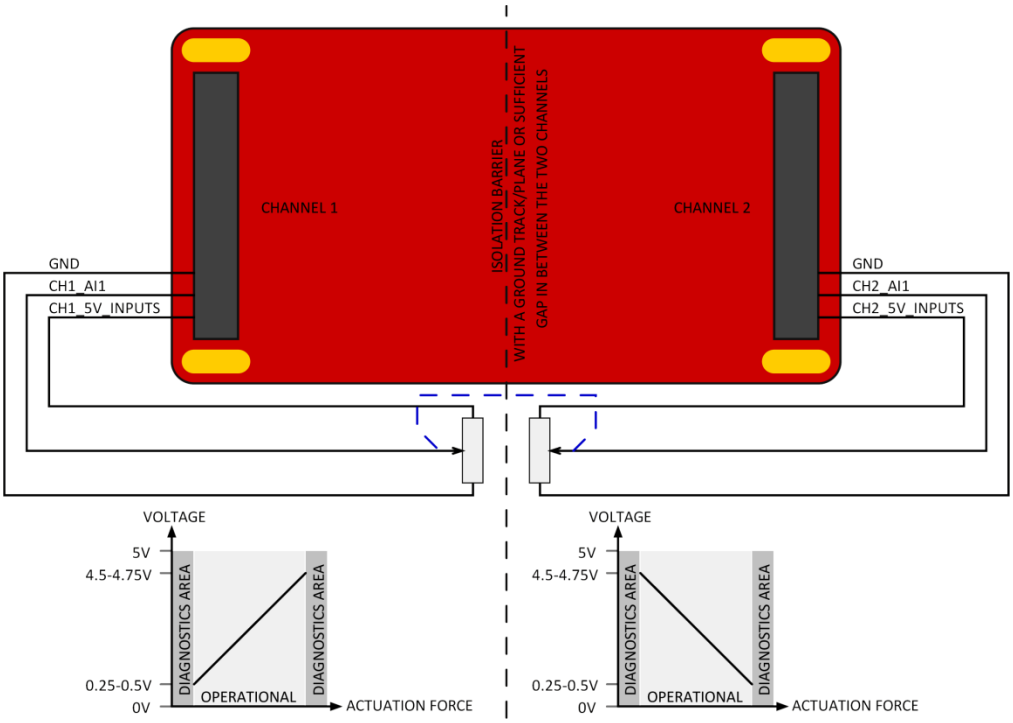
SREQ 0016	*Usage of sensor/switches without complementary outputs*
	Sensor/switches with identical output types **can** be used if the signal integrity from the redundant sensor/switches is guaranteed not to be affected by common cause failures. If uncertain, refer to ISO 13849-1/ISO 13849-2.

SREQ 0017	*Diagnostic band for analog sensors*
	Since short-circuit to ground and +5V can not be excluded, the operational voltage of each analog sensor shall be restricted to give room for a diagnostics band (typically 250-500mV). In the event of a sensor fault, one or both signal outputs shall rise to +5V **or** sink to GND.

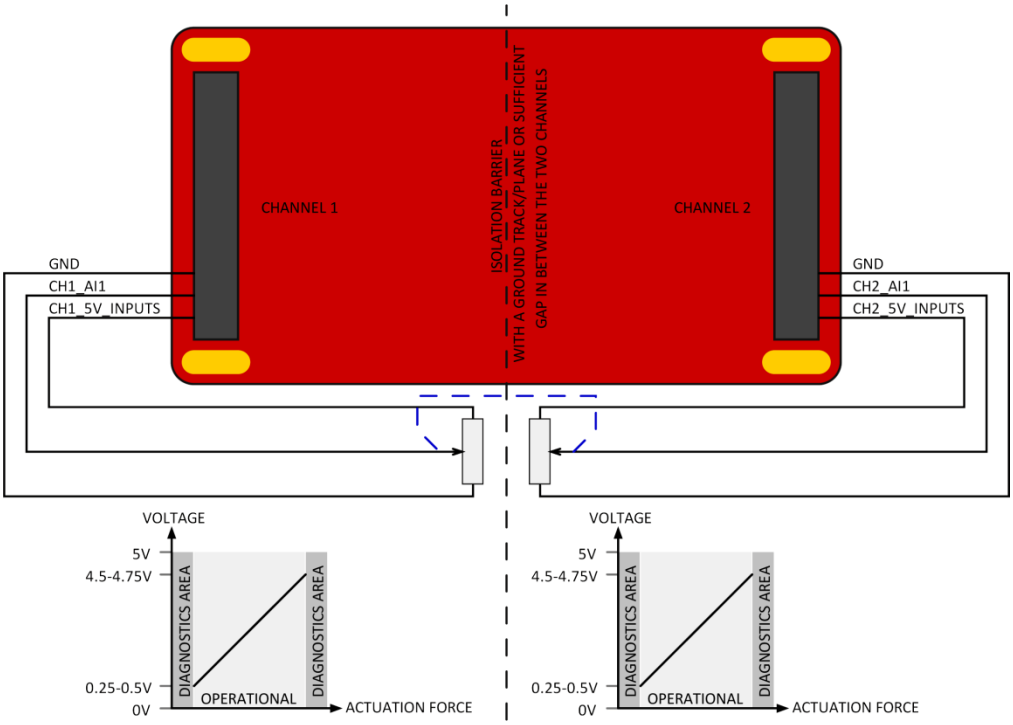
SREQ 0018	*CAN master runtime bootup evaluation*
	On bootup, the CAN master shall verify that the two redundant channels are in a safe-state (not-actuated). In the event of a failure the system shall be prevented from operating until the error has been resolved.

SREQ 0019	*CAN master runtime signal evaluation*
	The CAN master shall verify that the two redundant channels operate in a “linked” manner, the exact CAN master software implementation depends on the hardware structure of the sensor/switches.

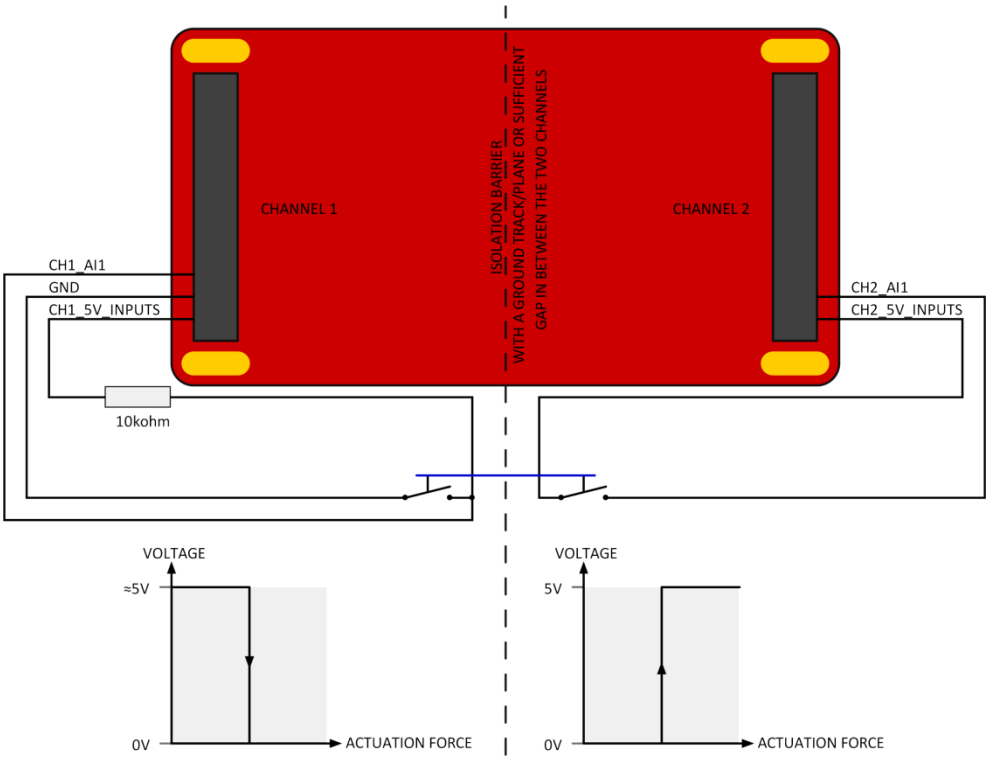
13.7.1 Safety connection of a fully redundant complementary analog sensor



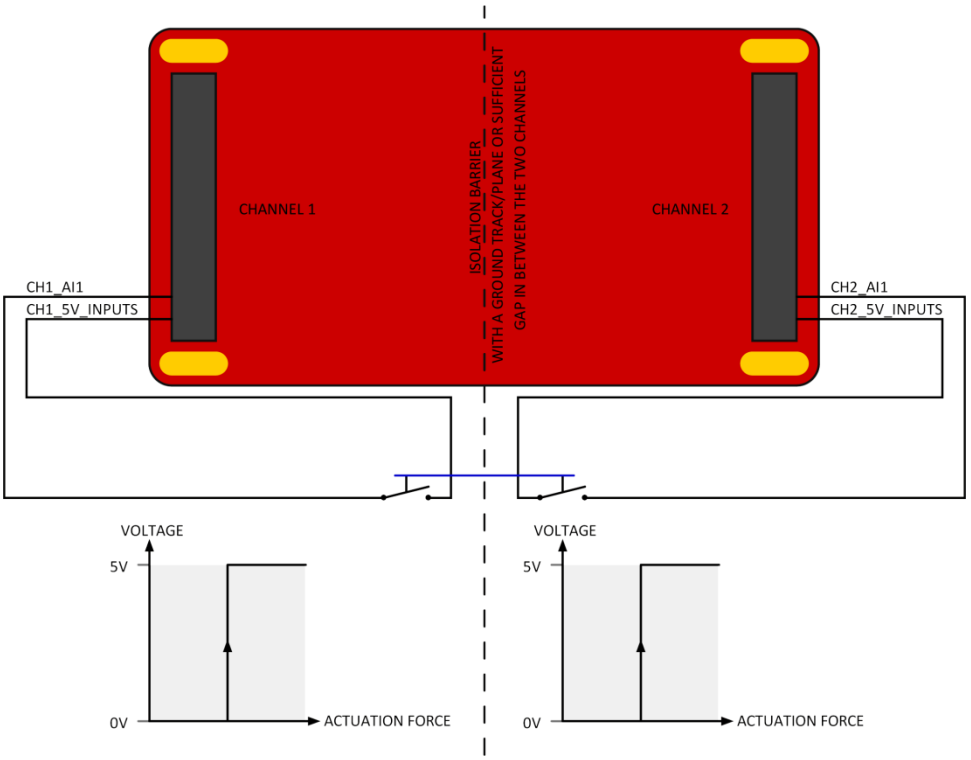
13.7.2 Safety connection of a fully redundant non-complementary analog sensor



13.7.3 Safety connection of a fully redundant complementary switch



13.7.4 Safety connection of a fully redundant non-complementary switch



14 PWM outputs

The SCM features a total of 20 digital outputs. Each CH**x**_DO**z** output is capable of sinking 1000mA. The entire SCM is capable of driving 2000mA in total on all outputs.
The digital output floats when the output is off and sinks to ground when active. Each digital output has an individually configurable PWM duty-cycle with 8bit resolution.
During the design phase of the mother-board the designer shall strive to balance the load on CH**x**_5V_OUTPUTS between each channel to avoid unnecessary component stress.

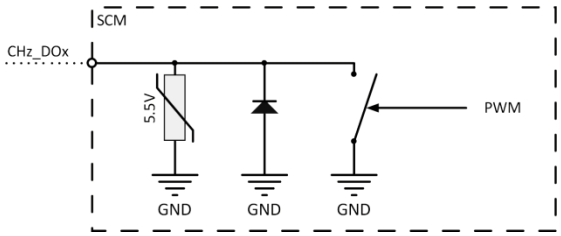
14.1 Safety note

The outputs on the SCM are not safety classified and shall not be used to control anything related to safety.

14.2 Short circuit protection

The PWM outputs are not short circuit protected. The short circuit protection is achieved due the use of short circuit protection on each +5V power-rail.

14.3 Internal diagram of a PWM output

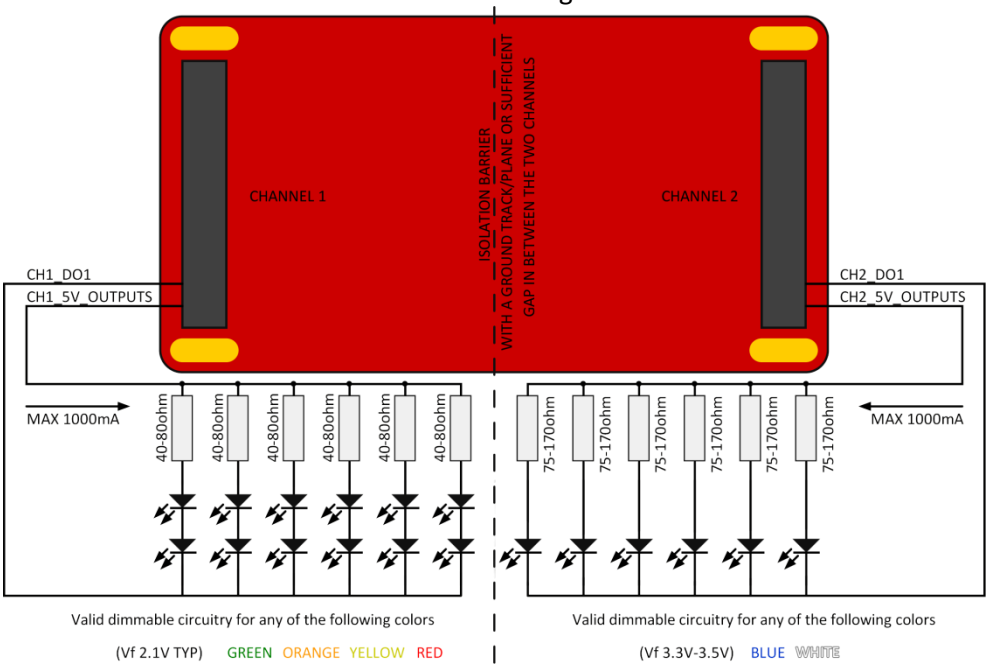


14.4 Example schematic

Please note that the schematics below are simplified and covers the typical applications which the SCM is intended for. The example covers the typical LED's available today. You should always read the data sheet for the actual LED in order to determine the actual forward voltage, maximum current vs life time and light intensity.
Theoretically 266 LED's (2.1Vf, 15mA) can be driven from a single SCM board. However one should always design for margins, and avoid designs which stress the components according to the maximum rated specification.

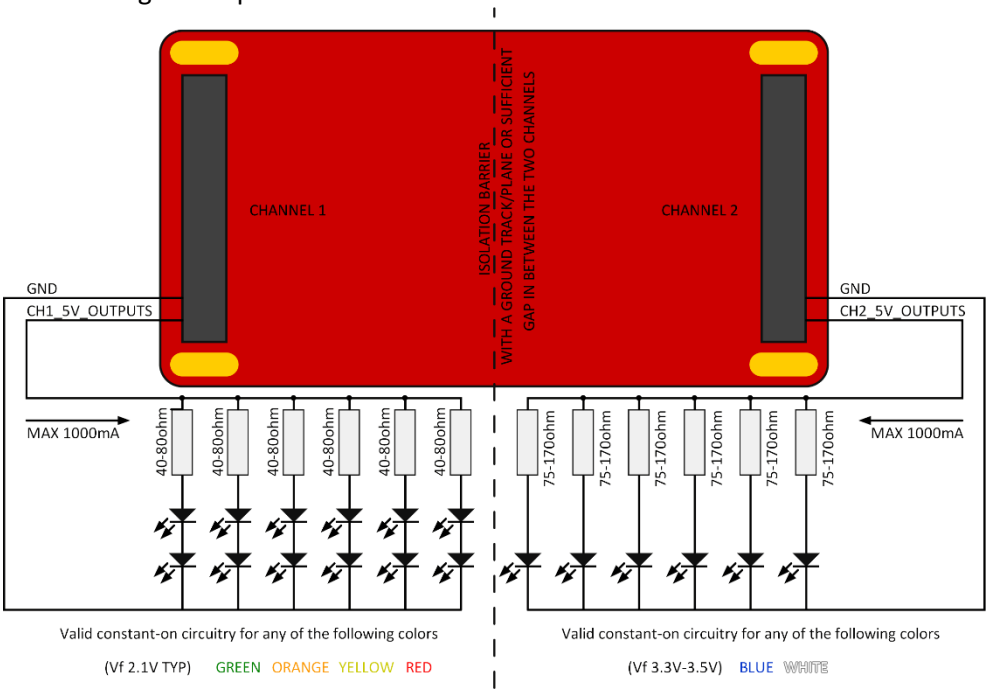
14.4.1 PWM dimmable LED's

The example below illustrates two individually dimmable LED blocks. If the maximum forward voltage drop of the LED's is larger than 2.4V the LED's has to be driven with a single current limiting resistor. If the maximum forward voltage drop is below 2.4V two LED's can be connected in series with one current limiting resistor.



14.4.2 Fixed-on LED's

For LED's which require constant on-time, consider connecting them to ground instead of a digital output. This will reduce the heat loss of the SCM and help to free up the number of available digital outputs.



15 SPI expansion ports

The SPI busses are intended to be connected to 75HC165 and/or 74HC595 in order to increase the number of I/O's on the PCB.

Please note that Electrum can not be held responsible for the signal integrity from the use of shift registers as this is heavily dependent on cable routing, cable length, earth plane, ESD protection etc. Customized SPI solutions shall always be verified with EMC testing.

15.1 ESD considerations

Care must be taken to protect the shift registers and SPI data lines from ESD. This document does not go into detail of how to do this.

15.2 RF interference considerations

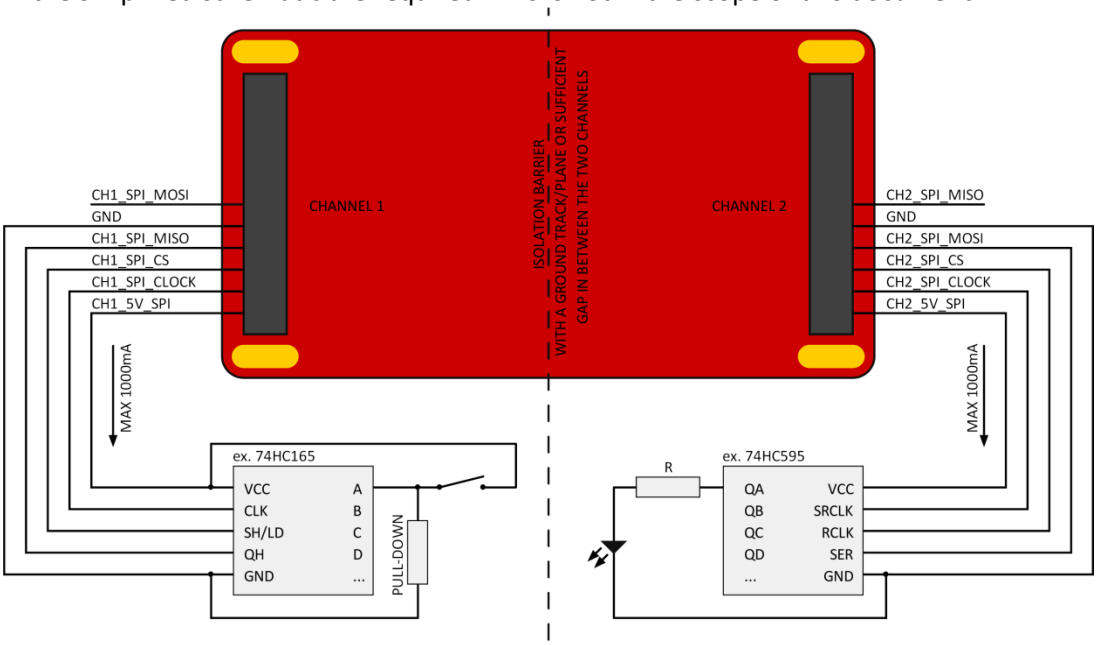
Care must be taken to verify that the shift registers and SPI data lines are sufficiently protected against RF interference. This document does not go into detail on how to do this.

15.3 Safety note

The SPI bus is not safety classified and shall **not** be used to transmit/receive any safety related signals.

15.4 Example schematic

Please note that the schematic below are simplified and covers the typical application which the SCM is intended for. More external components/connections other than those displayed in the simplified schematic are required. This is not in the scope of this document.



16 Node id inputs

The node id inputs are designed to be left unconnected (1) **or** connected to ground (0). No other electrical potential shall be connected to this input. Preferably 0 ohm resistors should be placed at the node-id inputs on the mother-board in order to easily configure the node-id of the SCM.

16.1 Input configuration vs J1939 Source Address

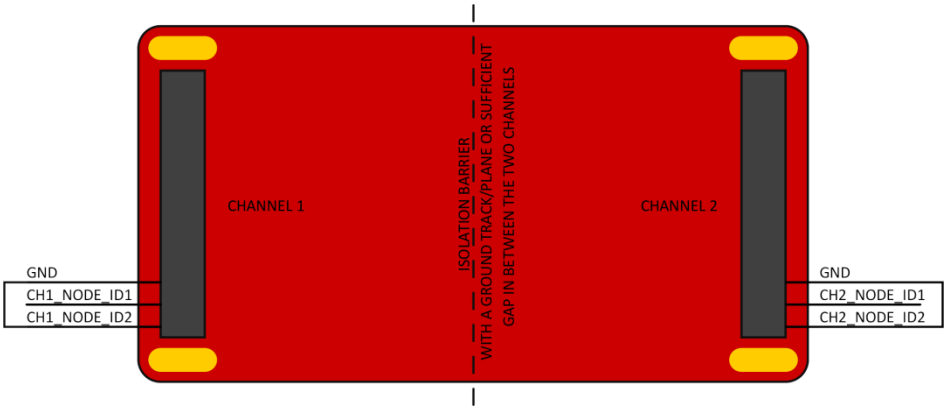
SREQ 0020	*Proper connection of node-id inputs*
	For safety reasons, channel 1 and channel 2 shall have an identical node-id configuration, otherwise the board is prevented from booting.

J1939 Source Address		CH1_NODE_ID1	CH1_NODE_ID2	CH2_NODE_ID1	CH2_NODE_ID2
Channel 1	Channel 2				
60	61	0	0	0	0
Invalid configuration		0	0	0	1
Invalid configuration		0	0	1	0
Invalid configuration		0	0	1	1
Invalid configuration		0	1	0	0
64	65	0	1	0	1
Invalid configuration		0	1	1	0
Invalid configuration		0	1	1	1
Invalid configuration		1	0	0	0
Invalid configuration		1	0	0	1
62	63	1	0	1	0
Invalid configuration		1	0	1	1
Invalid configuration		1	1	0	0
Invalid configuration		1	1	0	1
Invalid configuration		1	1	1	0
66	67	1	1	1	1

16.2 Example schematic

In this example, the node id is defined as follows (resulting in a source address of 62 and 63):

Pin identification	Pin value
CH1_NODE_ID1	1
CH1_NODE_ID2	0
CH2_NODE_ID1	1
CH2_NODE_ID2	0



17 CAN bus

The SCM supports CAN 2.0A, CAN 2.0B and CAN FD. The SCM communicates using CAN 2.0B as specified in SAE J1939.

17.1 CAN Bit rate

The SCM communicates using 250kbit/s bit-rate.

17.2 CAN termination

The SCM is **not** equipped with a CAN termination resistor. If the system requires a CAN termination in proximity to the SCM board, a CAN termination resistor should be placed on the mother-board or external wire harness.

18 Supply voltage

The SCM is suitable for both +12V and +24V applications. Some degradation of the device can occur during cold-crank in +12V systems. But the SCM operation is automatically restored once the system voltage settles again.

18.1 Restricted use of VBB inside assembly

The system voltage (VBB) should be limited to supplying the SCM board in the final assembly. No input except for CAN and VBB on the SCM board has overvoltage protection against +24V.
The supply voltage connector which mates with the mother-board should be chosen for uniqueness so that it can not by mistake or intent be mated with any low-voltage connector in the assembly.

SREQ 0021	***Overvoltage prevention***
	All I/O except for CAN and VBB shall be protected against overvoltage, otherwise the safety integrity of the SCM module can not be guaranteed. The supply voltage connector which mates with the mother-board should be chosen for uniqueness so that it can not by mistake or intent be mated with any low-voltage connector in the assembly.

19 Speaker

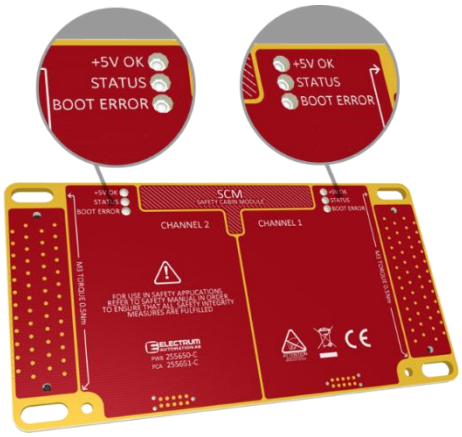
The SCM features a built-in speaker which can be used to alert the user in certain scenarios. The speaker has a fixed frequency of 2.73 kHz. The sound is controllable in an on/off manner.
The sound pressure level is 90dBa measured at 10cm distance in open air.

20 Status LED's

Each channel has 3 individual LED's used to indicate the SCM status. These LED's are not normally presented to the end-user but rather a means of diagnostics tool for technicians.

The LED's are located so that they are viewable even when the SCM board is mounted in a board-to-board configuration.

In the event where multiple errors are active at the same time, the error with the lowest amount of flashes will be prioritized.



LED		Description	
	+5V	On	Channel has supply voltage, however not necessarily +5V since this LED is connected directly between GND and +CH**x**_5V.
		Off	Channel does not have a supply voltage.
	Status	On/Off 50%	Channel fully operational. No error detected.
		Off	Error: The microprocessor in the corresponding channel has detected an error and is unable to safely start the program. Possible faults: • FLASH CRC/ECC error • EEPROM CRC/ECC error • RAM ECC error • Hardware failure • UNIT_ID inputs hardware read error
		1 flash	Error: Internal SPI communication error detected at least once. The error will remain until the power is cycled.
		2 flashes	Error: ADC error detected. The error will remain until the power is cycled.
		3 flashes	Error: CAN error passive or bus off detected. The error will remain until the power is cycled.
		4 flashes	Error: Internal watchdog timeout detected. The error will remain until the power is cycled.
		5 flashes	Error: CHx_5V_xxxx supply rail failure detected at least once. The error will remain until the power is cycled.
		6 flashes	Error: CAN SA conflict detected. Someone else is transmitting data on the CAN identifier which the SCM is transmitting on. The error will remain until the power is cycled.
		7 flashes	Error: CAN RX or TX overrun detected. The error will remain until the power is cycled.
		8 flashes	Error: CAN CRC32 checksum or CNT counter conflict detected. The error will remain until the power is cycled.
	Boot Error	Off	The microprocessor in the corresponding channel has booted properly.
		On	The microprocessor in the corresponding channel is unable to boot. Please note that the boot error LED be on during power-up, but once the application is successfully started the LED will be set to the off-state.

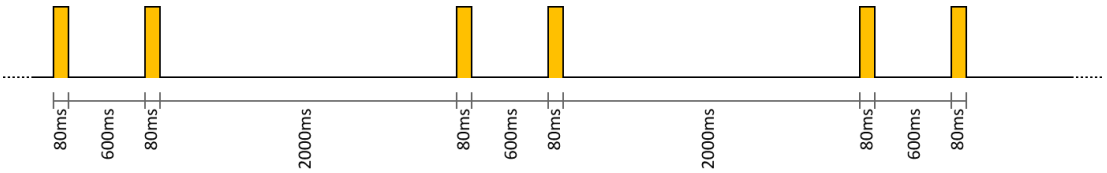
20.1 Status LED flash pattern

20.1.1 Led on/off illustration

When no error is present, the status LED will toggle on and off with a 1 second interval. In this mode the LED is synchronized between the two channels.

20.1.2 Led flash illustration

If an error occurs the status LED will flash a fixed number of times. The exact number of flashes depends on which error is present. In this illustration the LED flashes twice indicating that an ADC failure has been detected at least once.

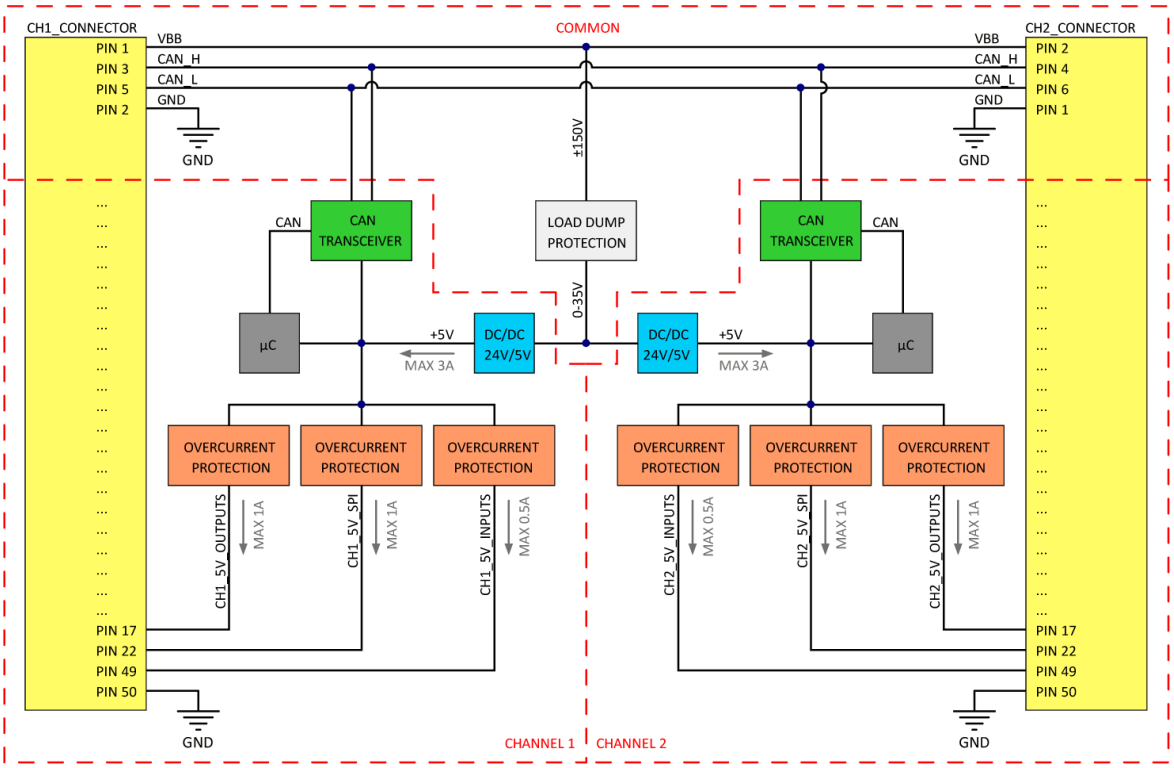


21 Power distribution block diagram

The common wires (VBB, CAN and GND) are internally connected to each other because it is argued that a dangerous common cause error is very unlikely to occur if any of these wires were to fail.

All GND pins are connected to the same potential. In other words, channel 1 and channel 2 share the same ground.

Please note however that all signals with a CH**z**_ prefix shall be protected against short circuit with the counterpart channel block **and** common block.



22 Connectors

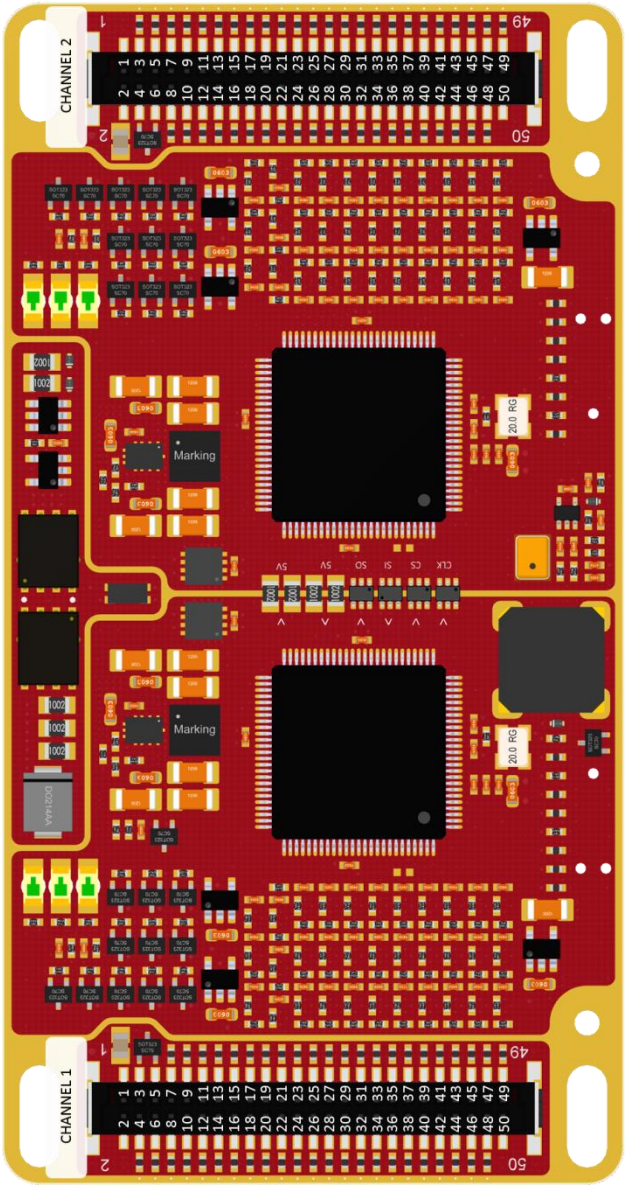
The circuit board features two connectors intended for board-to-board connection using two matching Harting HAR-flex 50p Female connectors (SMD or PTH).
The pin-out of each connector features the same set of redundant signals, please note however that the actual pin-out of each connector differs slightly in order to achieve a better PCB track routing.

22.1 Unused connector pins

For optimal EMC behaviour, it is recommended to connect all unused I/O pins to ground.
The following pins should be tied to ground if unused:

- CH**z**_AI**x**
- CH**z**_DO**x**
- CH**z**_SPI_MISO

22.2 Pin enumeration



22.3 Pin description Channel 1

Channel	Pin number	Pin identifier	Common	Note
1	1	VBB	x	+24V nominal
1	2	GND	x	Ground
1	3	CANH	x	CAN bus high
1	4	CH1_NODE_ID1		J1939 source address input
1	5	CANL	x	CAN bus low
1	6	CH1_NODE_ID2		J1939 source address input
1	7	CH1_DO1		Low-side PWM switch
1	8	CH1_DO2		Low-side PWM switch
1	9	CH1_DO3		Low-side PWM switch
1	10	CH1_DO4		Low-side PWM switch
1	11	CH1_DO5		Low-side PWM switch
1	12	CH1_DO6		Low-side PWM switch
1	13	CH1_DO7		Low-side PWM switch
1	14	CH1_DO8		Low-side PWM switch
1	15	CH1_DO9		Low-side PWM switch
1	16	CH1_DO10		Low-side PWM switch
1	17	CH1_5V_OUTPUTS		+5V output @ 1000mA
1	18	CH1_SPI_CS		SPI chip select
1	19	CH1_SPI_CLOCK		SPI clock
1	20	CH1_SPI_MISO		SPI master input, slave output
1	21	CH1_SPI_MOSI		SPI master output, slave input
1	22	CH1_5V_SPI		+5V output @ 1000mA
1	23	CH1_AI1		Analog/digital input
1	24	CH1_AI2		Analog/digital input
1	25	CH1_AI3		Analog/digital input
1	26	CH1_AI4		Analog/digital input
1	27	CH1_AI5		Analog/digital input
1	28	CH1_AI6		Analog/digital input
1	29	CH1_AI7		Analog/digital input
1	30	CH1_AI8		Analog/digital input
1	31	CH1_AI9		Analog/digital input
1	32	CH1_AI10		Analog/digital input
1	33	CH1_AI11		Analog/digital input
1	34	CH1_AI12		Analog/digital input
1	35	CH1_AI13		Analog/digital input
1	36	CH1_AI14		Analog/digital input
1	37	CH1_AI15		Analog/digital input
1	38	CH1_AI16		Analog/digital input
1	39	CH1_AI17		Analog/digital input
1	40	CH1_AI18		Analog/digital input
1	41	CH1_AI19		Analog/digital input
1	42	CH1_AI20		Analog/digital input
1	43	CH1_AI21		Analog/digital input
1	44	CH1_AI22		Analog/digital input
1	45	CH1_AI23		Analog/digital input
1	46	CH1_AI24		Analog/digital input
1	47	CH1_AI25		Analog/digital input
1	48	CH1_AI26		Analog/digital input
1	49	CH1_5V_INPUTS		+5V output @ 500mA
1	50	GND	x	Ground
1	Solder tab	GND	x	Ground

22.4 Pin description Channel 2

Channel	Pin number	Pin identifier	Common	Note
2	1	GND	x	Ground
2	2	VBB	x	+24V nominal
2	3	CH2_NODE_ID1		J1939 source address input
2	4	CANH	x	CAN bus high
2	5	CH2_NODE_ID2		J1939 source address input
2	6	CANL	x	CAN bus low
2	7	CH2_DO1		Low-side PWM switch
2	8	CH2_DO2		Low-side PWM switch
2	9	CH2_DO3		Low-side PWM switch
2	10	CH2_DO4		Low-side PWM switch
2	11	CH2_DO5		Low-side PWM switch
2	12	CH2_DO6		Low-side PWM switch
2	13	CH2_DO7		Low-side PWM switch
2	14	CH2_DO8		Low-side PWM switch
2	15	CH2_DO9		Low-side PWM switch
2	16	CH2_DO10		Low-side PWM switch
2	17	CH2_5V_OUTPUTS		+5V output @ 1000mA
2	18	CH2_SPI_CS		SPI chip select
2	19	CH2_SPI_CLOCK		SPI clock
2	20	CH2_SPI_MISO		SPI master input, slave output
2	21	CH2_SPI_MOSI		SPI master output, slave input
2	22	CH2_5V_SPI		+5V output @ 1000mA
2	23	CH2_AI1		Analog/digital input
2	24	CH2_AI2		Analog/digital input
2	25	CH2_AI3		Analog/digital input
2	26	CH2_AI4		Analog/digital input
2	27	CH2_AI5		Analog/digital input
2	28	CH2_AI6		Analog/digital input
2	29	CH2_AI7		Analog/digital input
2	30	CH2_AI8		Analog/digital input
2	31	CH2_AI9		Analog/digital input
2	32	CH2_AI10		Analog/digital input
2	33	CH2_AI11		Analog/digital input
2	34	CH2_AI12		Analog/digital input
2	35	CH2_AI13		Analog/digital input
2	36	CH2_AI14		Analog/digital input
2	37	CH2_AI15		Analog/digital input
2	38	CH2_AI16		Analog/digital input
2	39	CH2_AI17		Analog/digital input
2	40	CH2_AI18		Analog/digital input
2	41	CH2_AI19		Analog/digital input
2	42	CH2_AI20		Analog/digital input
2	43	CH2_AI21		Analog/digital input
2	44	CH2_AI22		Analog/digital input
2	45	CH2_AI23		Analog/digital input
2	46	CH2_AI24		Analog/digital input
2	47	CH2_AI25		Analog/digital input
2	48	CH2_AI26		Analog/digital input
2	49	CH2_5V_INPUTS		+5V output @ 500mA
2	50	GND	x	Ground
2	Solder tab	GND	x	Ground

23 J1939 Protocol

23.1 Source address

The source address of the SCM board is configured using the node-id inputs on the board. A total of 4 different source addresses are available for the SCM module. For further information see topic Node id inputs.

23.2 Data alignment

6 bytes in each J1939 PGN are used to transmit and receive signals, the 2 remaining bytes are used for packet counter and CRC.
When placing bit mapped values into a CAN data byte, the least significant byte always refers to the lowest instance number.
Example: If CH1_DI1-8 is transmitted in data[0] and has a value of 0x01, this indicates that CH1_DI1 is high and CH1_DI2-8 is low.

When signals which are larger than 8 bits are transferred, the least significant bits are always transferred in the first CAN data byte (little endian).

Example based on the following dummy mapping:

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x12345678 + SA	1	TX	8	CH1_AI1-4						CVC	CRC

CH1_AI1 = 0x123
CH1_AI2 = 0x456
CH1_AI3 = 0x789
CH1_AI4 = 0xABC
CVC = 0x01
CRC = 0x55

	bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	Description
data[0]	0x23								$CH1_AI1_L$
data[1]	0x1					0x6			$CH1_AI1_h + CH1_AI2_L$
data[2]	0x45								$CH1_AI2_h$
data[3]	0x89								$CH1_AI3_L$
data[4]	0x7					0xC			$CH1_AI3_h + CH1_AI4_L$
data[5]	0xAB								$CH1_AI4_h$
data[6]	0x01								CVC
data[7]	0x55								CRC

23.3 Safety additions

The SCM utilize the SAE J1939 protocol with added safety features in order to comply with ISO 13849-1.

23.3.1 CAN bus buffers

The SCM utilizes a CAN protocol without individual message feedback, relying on the fact that no message is buffered for a substantial amount of time. No CAN gateway shall be connected in between the SCM and the CAN master. The CAN master shall have an RX buffer size which in combination with the SCM transmission rate does not lead to an unacceptable delay.
The CAN master shall verify that each PGN is sent according to the transmission rate specified in this datasheet. If a PGN timeout is detected, the content of the next PGN shall not be trusted until at least 3 consecutive PGN has been received within the correct time slot.

SREQ 0022	*No CAN gateway*
	No CAN gateway shall be connected in between the SCM and the CAN master. The CAN master shall have an RX buffer size which in combination with the SCM transmission rate does not lead to an unacceptable delay.

SREQ 0023	*Time slot validation*
	The CAN master shall verify that each PGN is sent according to the transmission rate specified in this datasheet. If a PGN timeout is detected, the content of the next PGN data shall not be trusted until **at least** 3 consecutive PGN has been received within the correct time slot.

23.3.2 CAN timeout

SREQ 0024	*CAN timeout*
	If a safety related J1939 PGN has not been received within the system safety response time, the CAN master shall be programmed to automatically transition into a safe state.

23.3.3 Packet counter, CVC

Every J1939 packet transmitted and received from/to the SCM module shall have an 8bit packet counter (cyclic validation counter). The packet counter will start count at 0x00 and increase with 1 for every packet sent. Upon overflow, the packet counter will transition from 0xFF to 0x00. The packet counter is placed in the second last CAN data byte (data[6]). The CAN master shall verify that the packet counter is increased with 1 for every received J1939 packet.
Each PGN shall have an independent packet counter.

SREQ 0025	*Packet counter validation*
	The CAN master shall verify that the packet counter is increased with 1 for every received J1939 packet.

23.3.4 CRC-8 SAE-J1850

Every J1939 packet transmitted and received from/to the SCM module shall have an 8bit CRC to guarantee data integrity. The CRC shall be placed in the last data byte of the CAN packet.

The CRC is calculated with the following input:

```
byte crcSource = {
   canIdentifier,
   canIdentifier >> 8,
   canIdentifier >> 16,
   canIdentifier >> 24,
   canData[0],
   canData[1],
   canData[2],
   canData[3],
   canData[4],
   canData[5],
   canData[6],
}
```

The seed value (initial CRC) for this calculation is set to 0x53. After the CRC operation, the CRC is XOR'ed with 0x67.
The crcSource byte array is put through the CRC8 calculation using the polynomial:
$x^8 + x^4 + x^3 + x^2 + 1$.

Example of calculated CRC value of two consecutive CAN packets using the following settings:
SAE-J1850 CRC-8 incl ID
Seed: 0x53
XOR: 0x67
CVC length: 8

ID	DLC	Data							
		0	1	2	3	4	5	6	7
0x18FF0027	8	0x00	0x00	0x00	0x00	0x00	0x00	CVC 0x01	CRC (0xE1)
0x18FF0027	8	0x00	0x00	0x00	0x00	0x00	0x00	CVC 0x02	CRC (0xC6)

SREQ 0026	*CRC validation*
	The CAN master shall verify the J1939 CRC for correctness before attempting to parse the actual data.

23.4 J1939 PGN

For PDU 2 packets the “Proprietary B” and “Proprietary B – page 1” address space is used.
For PDU 1 packets the “Proprietary configurable Message #...” address space is used.

Channel 1 will transmit PGN’s on data page 0 and channel 2 will use data page 1. This ensures that **at least** two identifier bits differ between channel 1 and channel 2, minimizing the risk of addressing faults.

Please note that the RX PGN (PDU2) are always enabled, whilst only TX PGN1 are enabled by default.

23.4.1 TX PGN1 - DI1-26, PGN enabled, error register

PGN1	
Transmission rate	20ms
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	0 (0x00)
Priority	6
Parameter Group Number	**Channel 1:** 65280 (0x00FF00) **Channel 2:** 130816 (0x01FF00)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0000 + CH1_SA	1	TX	8	CH1_DI 1-8	CH1_DI 9-16	CH1_DI 17-24	CH1_DI 25-26	CH1 PGN enabled	CH1 Error register	CVC	CRC
0x19FF0000 + CH2_SA	2	TX	8	CH2_DI 1-8	CH2_DI 9-16	CH2_DI 17-24	CH2_DI 25-26 + CH2_MIC	CH2 PGN enabled	CH2 Error register	CVC	CRC

23.4.1.1 DI1-26

CH**x**_DI1-26 refers to the digital interpretation of CH**x**_AI1-26. All CH**x**_DI**z** are bit mapped with the least significant bit corresponding to the lowest instance number.

23.4.1.2 CH2_MIC

Whilst channel 1 is equipped with a speaker, channel 2 is equipped with a microphone, tuned to detect the sound frequency of the speaker.
If the speaker is determined to be safety critical for the desired application, the CAN Master shall ensure that the microphone signal is '1' for as long as the speaker is '1', and to some degree '0' when the speaker is '0'.
Since the microphone is completely isolated from the speaker with no logic shared between them, the microphone can become active even when the speaker is not enabled, for example if there is a presence of high ambient sounds with a sufficiently high sound pressure level.
The CAN master shall incorporate a logic functionality which monitors that the microphone is '0', 90% of the total time which the speaker is '0'. Thus, introducing some fault tolerance against sound noise.
The microphone is only guaranteed to work when the speaker is enabled on maximum volume (0xFF).

23.4.1.3 CHx PGN enabled

PGN enabled is a bit mapped byte which reports the enabled state of PGN2-9. On power up, this byte defaults to 0, indicating that PGN2-9 is disabled.
Example: If "CH1 PGN enabled" is transmitted as 0x03, this indicates that CH1 PGN2 and CH1 PGN3 is **enabled** and CH1 PGN4-9 is **disabled**.
The software in the CAN master shall verify that the CH**x** PGN enabled corresponds to the desired setting upon every reception of PGN1. If the value does not match the expected value, a PGN10 shall be transmitted to the SCM module to reflect the desired setting.

23.4.1.4 CHx Error register

The error register is a bit mapped byte which is used to report potential errors to the CAN master. The error register is 0 when no error is present. Please note that multiple errors can be active at the same time.
Also note that the SCM module performs more diagnostics than the ones stored in the error register, but not all errors are not possible to report since the safety integrity can not be guaranteed if the module were to communicate on the CAN bus during the presence of these errors, for example flash CRC error.

Safety related	Error description	Error register	Error identifier
x	Source address conflict detected. Someone else is transmitting data using a CAN identifier which the SCM is transmitting on.	00000001	ERR_SA
x	Internal SPI communication error detected	00000010	ERR_SPI
x	Internal Clock error detected	00000100	ERR_CLOCK
x	Internal ADC **or** supply voltage error detected	00001000	ERR_ADC
x	CH**x**_5V_INPUTS error detected	00010000	ERR_5V_INPUTS
	CH**x**_5V_SPI error detected	00100000	ERR_5V_SPI
	CH**x**_5V_OUTPUTS error detected	01000000	ERR_5V_OUTPUTS
	CAN CRC checksum **or** CVC counter error detected	10000000	ERR_CAN_COM

SREQ 0027	*Error register interpretation*
	The CAN master shall be programmed to enter a safe state in case the SCM reports **one or several** error(s) which are categorised as safety related in the error register.

23.4.1.5 ERR_SA

The SCM continuously monitors **all** incoming CAN packets. If the SCM receives a CAN packet with a CAN identifier which it is responsible for transmitting (i.e. a “TX PGN1” packet) this error will be set. The error will remain until the power to the module has been cycled.
This error prevents SA addressing faults on the CAN bus.

23.4.1.6 ERR_SPI

The SCM continuously exchange data internally between Channel 1 and Channel 2 by using the SPI bus every 2ms. Each SPI packet has its own CRC-16 and 8 bit packet counter.
In case an internal SPI communication error is detected this flag will be set to 1 and stay 1 until the error has been resolved, which requires multiple, consecutive receptions of correct SPI packets.

23.4.1.7 ERR_CLOCK

The SCM continuously compares the internal clock (1µs resolution system tick timer) between the two channels by using the internal SPI bus. If the clock deviance is too large an error will be set.
Note that it is not possible to know which channel caused the error; it could be one or the

other, or both.
The error will be cleared automatically once a pre-defined number of consecutive clock compare tests have successfully been carried out by each channel.

23.4.1.8 ERR_ADC

This flag is the sum of two possible errors:

- Each channel in the SCM continuously monitors a reference voltage (bandgap voltage) in order to determine that the ADC is working correctly. If the ADC sample of the bandgap voltage (typically 1V) is outside of the tolerated voltage window, the ERR_ADC flag will be set and not cleared until the voltage is inside the tolerated voltage window again.
- Each channel in the SCM continuously monitors the +5V supply of the counterpart channel. In case the counterpart +5V supply is outside the tolerated voltage window, the ERR_ADC flag will be set and not cleared until the voltage is inside the tolerated voltage window again.

23.4.1.9 ERR_5V_INPUTS

Each channel in the SCM continuously monitors its own +5V supply which is used to supply voltage to external switches and sensors.
In case the CH**x**_5V_SUPPLY_INPUTS is outside the tolerated voltage window, the ERR_ 5V_INPUTS flag will be set and not cleared until the voltage is inside the tolerated voltage window again.

23.4.1.10 ERR_5V_SPI

Each channel in the SCM continuously monitors its own +5V supply which is used to supply voltage to external SPI devices
In case the CH**x**_5V_SUPPLY_SPI is outside the tolerated voltage window, the ERR_ 5V_SPI flag will be set and not cleared until the voltage is inside the tolerated voltage window again.

23.4.1.11 ERR_5V_OUTPUTS

Each channel in the SCM continuously monitors its own +5V supply which is used to supply voltage to external LED's.
In case the CH**x**_5V_SUPPLY_OUTPUTS is outside the tolerated voltage window, the ERR_ 5V_OUTPUTS flag will be set and not cleared until the voltage is inside the tolerated voltage window again.

23.4.1.12 ERR_CAN_COM

The SCM continuously monitors **all** incoming J1939 CAN packets which is addressed to the SCM. If the SCM detects an invalid CRC **or** CNT value this error will be set. The error will remain until the power to the module has been cycled.

23.4.2 TX PGN2 - AI1-4

PGN2	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	1 (0x01)
Priority	6
Parameter Group Number	**Channel 1:** 65281 (0x00FF01) **Channel 2:** 130817 (0x01FF01)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0100 + CH1_SA	1	TX	8	CH1_AI1-4						CVC	CRC
0x19FF0100 + CH2_SA	2	TX	8	CH2_AI1-4						CVC	CRC

23.4.3 TX PGN3 - AI5-8

PGN3	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	2 (0x02)
Priority	6
Parameter Group Number	**Channel 1:** 65282 (0x00FF02) **Channel 2:** 130818 (0x01FF02)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0200 + CH1_SA	1	TX	8	CH1_AI5-8						CVC	CRC
0x19FF0200 + CH2_SA	2	TX	8	CH2_AI5-8						CVC	CRC

23.4.4 TX PGN4 - AI9-12

PGN4	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	3 (0x03)
Priority	6
Parameter Group Number	**Channel 1:** 65283 (0x00FF03) **Channel 2:** 130819 (0x01FF03)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0300 + CH1_SA	1	TX	8	CH1_AI9-12						CVC	CRC
0x19FF0300 + CH2_SA	2	TX	8	CH2_AI9-12						CVC	CRC

23.4.5 TX PGN5 - AI13-16

PGN5	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	4 (0x04)
Priority	6
Parameter Group Number	**Channel 1:** 65284 (0x00FF04) **Channel 2:** 130820 (0x01FF04)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0400 + CH1_SA	1	TX	8	CH1_AI13-16						CVC	CRC
0x19FF0400 + CH2_SA	2	TX	8	CH2_AI13-16						CVC	CRC

23.4.6 TX PGN6 - AI17-20

PGN6	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	5 (0x05)
Priority	6
Parameter Group Number	**Channel 1:** 65285 (0x00FF05) **Channel 2:** 130821 (0x01FF05)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0500 + CH1_SA	1	TX	8	CH1_AI17-20						CVC	CRC
0x19FF0500 + CH2_SA	2	TX	8	CH2_AI17-20						CVC	CRC

23.4.7 TX PGN7 - AI21-24

PGN7	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	6 (0x06)
Priority	6
Parameter Group Number	**Channel 1:** 65286 (0x00FF06) **Channel 2:** 130822 (0x01FF06)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0600 + CH1_SA	1	TX	8	CH1_AI21-24						CVC	CRC
0x19FF0600 + CH2_SA	2	TX	8	CH2_AI21-24						CVC	CRC

23.4.8 TX PGN8 - AI25-26, +VBB supply voltage

PGN8	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	7 (0x07)
Priority	6
Parameter Group Number	**Channel 1:** 65287 (0x00FF07) **Channel 2:** 130823 (0x01FF07)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0700 + CH1_SA	1	TX	8	CH1_AI25-26			+VBB Supply voltage		0x00(1)	CVC	CRC
0x19FF0700 + CH2_SA	2	TX	8	CH2_AI25-26			0x00(1)	0x00(1)	0x00(1)	CVC	CRC

Note: 1. Reserved for future use. 0x00 is used to indicate unused data bytes.

23.4.8.1 +VBB Supply voltage

The supply voltage is reported as a 16bit unsigned integer, 0-65535mV. Please note that only channel 1 has the capability to report the +VBB supply voltage.

23.4.9 TX PGN9 - SPI input

The SCM module supports a maximum of 6pcs of 8-bit shift registers per SPI bus (74HC165). Resulting in a total of 48 SPI clock cycles per chip select.
The result from the first shift register will be placed in data[0], the next in line will be placed in data[1] and so on.

PGN9	
Transmission rate	20ms (when enabled)
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	8 (0x08)
Priority	6
Parameter Group Number	**Channel 1:** 65288 (0x00FF08) **Channel 2:** 130824 (0x01FF08)
Enabled	**Disabled on bootup**

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0800 + CH1_SA	1	TX	8	CH1_SPI_DATA-IN						CVC	CRC
0x19FF0800 + CH2_SA	2	TX	8	CH2_SPI_DATA-IN						CVC	CRC

23.4.10 RX PGN10 - PGN enabled, PWM transition time

PGN10	
Data length	8 bytes
Data page	0
PDU format	177 (0xB1)
PDU specific	Destination adress (CH1_SA or CH2_SA)
Priority	7
Parameter Group Number	45312 (0x00B100)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x1CB10000 + (CH1_SA<<8) + SA$^{CAN-MASTER}$	1	RX	8	CH1 PGN Enabled	CH1 PWM Transition time	0x00[1]	0x00[1]	0x00[1]	0x00[1]	CVC	CRC
0x1CB10000 + (CH2_SA<<8) + SA$^{CAN-MASTER}$	2	RX	8	CH2 PGN Enabled	CH2 PWM Transition time	0x00[1]	0x00[1]	0x00[1]	0x00[1]	CVC	CRC

Note: 1. Reserved for future use. 0x00 is used to indicate unused data bytes.

23.4.10.1 CHx PGN Enabled

PGN enabled is a bit mapped byte which sets the enabled state of PGN2-9. On power up, this byte defaults to 0, indicating that PGN2-9 is disabled. The state of this byte is always reported in PGN1.
Example: If “CH1 PGN enabled” is set to 0x03, CH1 PGN2 and CH1 PGN3 will become enabled and CH1 PGN4-9 disabled.

23.4.10.2 CHx PWM transition time

Set to 0 by default. If the value is set to 0, the requested PWM duty-cycle will be applied directly without a transition. If this value differs from 0, this value will become a millisecond*10 transition timer.

Example:
Set the CH1 PWM transition time to 5.
Assume that the previous PWM duty-cycle of CH1_DO1 is 0x00.
Set the PWM duty-cycle of CH1_DO1 to 0xFF.
The CH1_DO1 PWM duty-cycle will now exponentially transition from 0x00 -> 0xFF over a period of 50ms.

This feature is suitable when LED’s are driven from the PWM outputs, this will enable all on/off toggling of LED’s to have a nice fade-in, fade-out effect.
This feature is implemented to reduce the CAN bus load in cases where PWM transitions are desired.

23.4.11 RX PGN11 - CHx_DO1-6

PGN11	
Data length	8 bytes
Data page	0
PDU format	178 (0xB2)
PDU specific	Destination adress (CH1_SA or CH2_SA)
Priority	7
Parameter Group Number	45568 (0x00B200)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x1CB20000 + (CH1_SA<<8) + SA$^{CAN-MASTER}$	1	RX	8	CH1_ DO1 DC	CH1_ DO2 DC	CH1_ DO3 DC	CH1_ DO4 DC	CH1_ DO5 DC	CH1_ DO6 DC	CVC	CRC
0x1CB20000 + (CH2_SA<<8) + SA$^{CAN-MASTER}$	2	RX	8	CH2_ DO1 DC	CH2_ DO2 DC	CH2_ DO3 DC	CH2_ DO4 DC	CH2_ DO5 DC	CH2_ DO6 DC	CVC	CRC

23.4.11.1 CHx_DOz Duty-Cycle

The PWM duty-cycle is configurable between 0x00 to 0xFF. 0x00 defines the state where the digital output is fully off and 0xFF represents fully on.

23.4.11.2 Timeout

The CAN master must make sure to update PGN11 with a **minimum** interval of 2000ms. If the SCM detects that no PGN11 has been received for 2500ms, all corresponding outputs will be disabled (= set to 0).

23.4.12 RX PGN12 - CHx_DO7-10, Speaker enable

PGN12	
Data length	8 bytes
Data page	0
PDU format	179 (0xB3)
PDU specific	Destination adress (CH1_SA or CH2_SA)
Priority	7
Parameter Group Number	45824 (0x00B300)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x1CB30000 + (CH1_SA<<8) + SA$^{CAN-MASTER}$	1	RX	8	CH1_ DO7 DC	CH1_ DO8 DC	CH1_ DO9 DC	CH1_ DO10 DC	Speaker Enable	Speaker Volume	CVC	CRC
0x1CB30000 + (CH2_SA<<8) + SA$^{CAN-MASTER}$	2	RX	8	CH2_ DO7 DC	CH2_ DO8 DC	CH2_ DO9 DC	CH2_ DO10 DC	0x00(1)	0x00(1)	CVC	CRC

Note: 1. Reserved for future use. 0x00 shall be used to indicate reserved data bytes.

23.4.12.1 Timeout

The CAN master must make sure to update PGN12 with a **minimum** interval of 2000ms. If the SCM detects that no PGN12 has been received for 2500ms, all corresponding outputs and speaker will be disabled (= set to 0).

23.4.12.2 CHx_DOz Duty-Cycle

The PWM duty-cycle is configurable between 0x00 to 0xFF. 0x00 defines the state where the digital output is fully off and 0xFF represents fully on.

23.4.12.3 Speaker Enable

Controls the speaker on the SCM board. Valid data range 0-255. See table below for further description.

Speaker enable description	
0	Speaker off. No sound is generated
1	Speaker continuously on until speaker enable is updated or a CAN timeout occurs.
2-255	Speaker will toggle between on and off state with the time written to speaker enable (20-2550 milliseconds)

23.4.12.4 Speaker Volume

Controls the volume of the speaker on the SCM board once it is turned on.
Valid data range 0-255. Please note that speaker enable has to be larger than 0 in order for the SCM to produce a sound. See table below for further description.

Speaker volume description	
0	Lowest volume. Not audible.
255	Maximum volume.

23.4.13 RX PGN13 - SPI output

The SCM module supports a maximum of 6pcs of 8-bit shift registers per SPI bus (74HC595). Resulting in a total of 48 SPI clock cycles per chip select.
If only one shift register is used, the data should be placed in data[0], if two shift registers are used data[0] and data[1] should be used, and so on…

PGN13	
Data length	8 bytes
Data page	0
PDU format	180 (0xB4)
PDU specific	Destination adress (CH1_SA or CH2_SA)
Priority	7
Parameter Group Number	46080 (0x00B400)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x1CB40000 + (CH1_SA<<8) + SA$^{CAN-MASTER}$	1	RX	8	CH1_SPI_DATA-OUT						CVC	CRC
0x1CB40000 + (CH2_SA<<8) + SA$^{CAN-MASTER}$	2	RX	8	CH2_SPI_DATA-OUT						CVC	CRC

23.4.14 TX PGN14 - SW & HW Versions

It is possible to read the software version for the bootloader and application. The software version is reported as 3 bytes, i.e. [1,2,3], representing the version “1.2.3”.
The initial version will have software version “1.0.0”.
The hardware version is reported in ASCII format, starting count at character ‘A’. Please note that the hardware version for both channel 1 and channel 2 are equal to each other as they reside on the same PCB board.
It is recommended to read the versions during bootup and present them to the user using a suitable HMI in order to enhance the troubleshooting capability of the overall system.
Please note that this PGN will be sent once during bootup. If retransmission is desired, a request PGN message must be sent.

PGN14	
Transmission rate	On bootup and on request
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	13 (0x0D)
Priority	6
Parameter Group Number	**Channel 1:** 65293 (0x00FF0D) **Channel 2:** 130829 (0x01FF0D)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0D00 + CH1_SA	1	TX	8	Channel 1 application version			Channel 1 bootloader version			Hardware version	CRC
0x19FF0D00 + CH2_SA	2	TX	8	Channel 2 application version			Channel 2 bootloader version			Hardware version	CRC

23.4.15 TX PGN15 - Application information

This is mainly used during production, but can also be relevant for troubleshooting.
This PGN is used to read the checksum and identifier of the application. The checksum is a 32bit CRC. The application identifier is a 27xxxx number used to identify the application firmware which is loaded in the SCM module. Please note that this PGN will be sent once during bootup. If retransmission is desired, a request PGN message must be sent.

PGN15	
Transmission rate	On bootup and on request
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	14 (0x0E)
Priority	6
Parameter Group Number	**Channel 1:** 65294 (0x00FF0E) **Channel 2:** 130830 (0x01FF0E)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0E00 + CH1_SA	1	TX	8	Channel 1 Application CRC				Channel 1 Application identifier			CRC
0x19FF0E00 + CH2_SA	2	TX	8	Channel 2 Application CRC				Channel 2 Application identifier			CRC

23.4.16 TX PGN16 - Bootloader information

This is mainly used during production, but can also be relevant for troubleshooting.
This PGN is used to read the checksum and identifier of the bootloader. The checksum is a 32bit CRC. The bootloader identifier is a 27xxxx number used to identify the bootloader which is loaded in the SCM module. Please note that this PGN will be sent once during bootup. If retransmission is desired, a request PGN message must be sent.

PGN16	
Transmission rate	On bootup and on request
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	15 (0x0F)
Priority	6
Parameter Group Number	**Channel 1:** 65295 (0x00FF0F) **Channel 2:** 130831 (0x01FF0F)
Enabled	Always enabled

ID	CH	DIR	DLC	Data							
				0	1	2	3	4	5	6	7
0x18FF0F00 + CH1_SA	1	TX	8	Channel 1 Bootloader CRC				Channel 1 Bootloader identifier			CRC
0x19FF0F00 + CH2_SA	2	TX	8	Channel 2 Bootloader CRC				Channel 2 Bootloader identifier			CRC

23.4.17 TX PGN17 - Error information

This PGN is mainly used during troubleshooting to get a better understanding of the root cause behind an error. This PGN shall not be used in any safety related function.
Please note that this PGN is only available on request.

PGN17	
Transmission rate	On request
Data length	8 bytes
Data page	**Channel 1:** 0 (0x0) **Channel 2:** 1 (0x1)
PDU format	255 (0xFF)
PDU specific	16 (0x10)
Priority	6
Parameter Group Number	**Channel 1:** 65296 (0x00FF10) **Channel 2:** 130832 (0x01FF10)
Enabled	Always enabled

ID	CH	DIR	DLC	Data						
				0	1	2	3	4	5	6	7
0x18FF1000 + CH1_SA	1	TX	8	Channel 1 CRC error counter	Channel 1 CVC error counter	Reserved					CRC
0x19FF1000 + CH2_SA	2	TX	8	Channel 2 CRC error counter	Channel 2 CVC error counter						CRC

23.4.18 RX Request PGN

The request PGN is used to force the SCM module to transmit a desired PGN. Please note that this is always valid for PGN 14-17 and the PGN 1-9 if the cyclic transmission rate is disabled.

Request PGN	
Data length	3 bytes
Data page	0
PDU format	234 (0xEA)
PDU specific	Destination adress (CH1_SA or CH2_SA)
Priority	6
Parameter Group Number	59904 (0x00EA00)
Enabled	Always enabled

ID	CH	DIR	DLC	Data		
				0	1	2
0x18EA0000 + (CH1_SA<<8) + $SA^{CAN-MASTER}$	1	RX	3	Requested PGN		
0x18EA0000 + (CH2_SA<<8) + $SA^{CAN-MASTER}$	2	RX	3	Requested PGN		

24 Declaration of conformity CE

Product name Product Description	SCM Safety Cabin module. CAN bus I/O module.
Manufacturer Address	Electrum Automation AB Industrivägen 8, 901 30 Umeå, Sweden

The undersigned hereby declares on behalf of Electrum Automation AB, that the above reference product, to which this declaration relates, complies with the essential requirements of the following applicable European Directives, and carries the CE marking accordingly:

2011/65/EU	As amended by (EU) 2015/863 – RoHS Directive
2006/42/EC	Machinery Directive
2014/30/EU	Electromagnetic Compatibility Directive

And conforms with the following Product Standards:

EN ISO 13849 1:2015 + A2:2020	Functional safety. (Performance Level d, Category 3)
EN ISO 13766 1:2018	Earth-moving and building construction machinery – EMC – Part 1: General requirements
EN ISO 13766 2:2018	Earth-moving and building construction machinery – EMC – Part 2: Additional requirements for functional safety
ISO 11452 2:2004	Radiated RF immunity
ISO 11452 4:2011	Bulk Current Injection (BCI)
ISO 7637 2:2011	Electrical transients on supply lines
ISO 10605:2008 + Cor1:2010 + A1:2014	Electrostatic discharge (ESD)
ISO 16750 2:2012	Electrical loads and supply disturbances
EN IEC 63000:2018	Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

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2026-06-17	Umeå, Sweden	
Date	Location	David Thomas QHSE Manager Electrum Automation AB

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26 Document history

Document revision	Description	Release date
A	• Initial release	2019-11-06
B	• Fixed typo in RX PGN 11-13 Parameter Group Number. Incorrect hexadecimal to decimal conversion.	2021-04-06
C	• Fixed description of voltage thresholds for digital inputs in order to match the actual software implementation. Previously 2400mV/2600mV, changed to 1750mV/3250mV. Modification tracked by modification notice MN-278.	2023-02-24
D	• Added section “Connector manufacturer” • Document redesigned using new document template.	2025-01-27
E	• Fixed formatting issues from redesign to new document template.	2025-02-21
F	• Clarified logic level 0/1 for node-id inputs • Updated declaration of conformity CE • Change the node ID result in 16.2 example to the correct ID	2026-06-23

27 Contact us

For more information, visit our website www.electrumab.se or contact us at info@electrumab.se.